Silicon Mini-Strip sensor for STAR Forward Tracking System Upgrade

The STAR collaboration is looking to perform physics measurements in polarized p-p and p-A runs starting from 2020 and e-p and e-A runs after 2025. These measurements can provide valuable information about nucleon spin structure. One of requirement of such a measurements is to detect and measure unidentified charged hadrons, identified hadrons ($\pi 0$, Λ), direct photons, e+e- pairs from Drell-Yan production, di-hadron/jet and photon-hadron/jet correlations measure at large rapidity regions ($2.5<\eta<4$). Through simulation studies () have shown that a Forward Tracking System (FTS) including three Silicon Mini-strip planes, by providing charge-sign separation through track curvatures and photon identification, can satisfy the requirements.

We started an R&D program to design and optimize a Silicon strip based FTS. The initial plan is developing Silicon mini-strip sensor and find proper readout front end following with assembling prototype and real beam tests. The time scale of completing the project is 1.5-2 years. Results of this project will be essential to complete detector system design by 2016. We already completed initial phase of project by designing the first version of sensor wafers and got the price quote from sensor manufacturer.

The sensor design is based on Single sided Double metal AC coupled Silicon mini-strip (P on N) in 3 size regards to location in detector which are at Z1@70CM, Z2@105CM, Z3@140 CM (Figure 1). The each sensor plane is divided to 12 wedge modules covering 2π range in φ. Each module contains 128 (φ) times 8 (η) strips (Figure 2-a). To reduce the material budget in the detector acceptance the frontend readout chips are located at the outer radius edge which all of them are connected to sensor strips via second metal layer tacks.

Each sensor wafer has 10 mask layers as following (Figure 2-b):

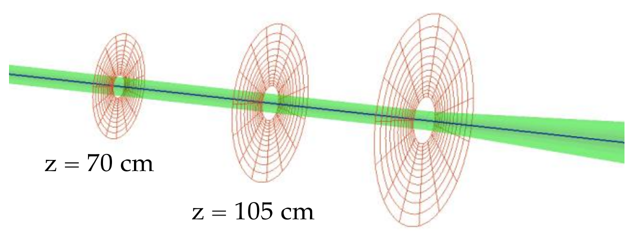

Figure 1 Layout of silicon sensor plates

1. Layer for Al layer at back-plane .
2. Layer for N++ Implant at back-plane.
3. Layer for N-Implant.
4. Layer for P-implant.
5. Layer for Poly-Silicon for Bias resistor.
6. Layer for Metal-layer 1 over SiO2 layer.
7. Layer for Metal Via 1 layer to connect P-implant to Poly-Silicon bias resistor.
8. Layer Metal layer 2 for routing to Bonding Pads at edge of wafer.
9. Layer for Metal Via 2 layer to Connect Metal-layer 1 to 2 .
10. Layer for Passive (protection) layer as negative mask.

Poly-Silicon layer resistor would be connected to P-Implant via Metal-Via1 and from the other side to Bias ring via direct epitaxial connection (bias ring is in Metal-layer 1) with value of 3MΩ and length of 100 µm. The width of Strips is constant 40 µm with AC couple Metal with an overhang length of 2 µm. The Width of strips and overhang metals could change regard to further investigation and simulation to optimize the efficiency of detector as well as number of needed Guard-rings. Also design rule check could vary regard to manufacturer specification. Design rules for routing tracks to readout chip and bond pads are as following:

- Track Clearance 10um
- Metal readout track is 10um.
- Between each sensor raw at R plane there is 140um gap to feed the Bias line trough.
- AC couple metal strip also are shorter about 100um than P-implant strip reserved for Poly-silicon Bias resistor.
- Bias line has track width of 40um and Guard-rings 50um

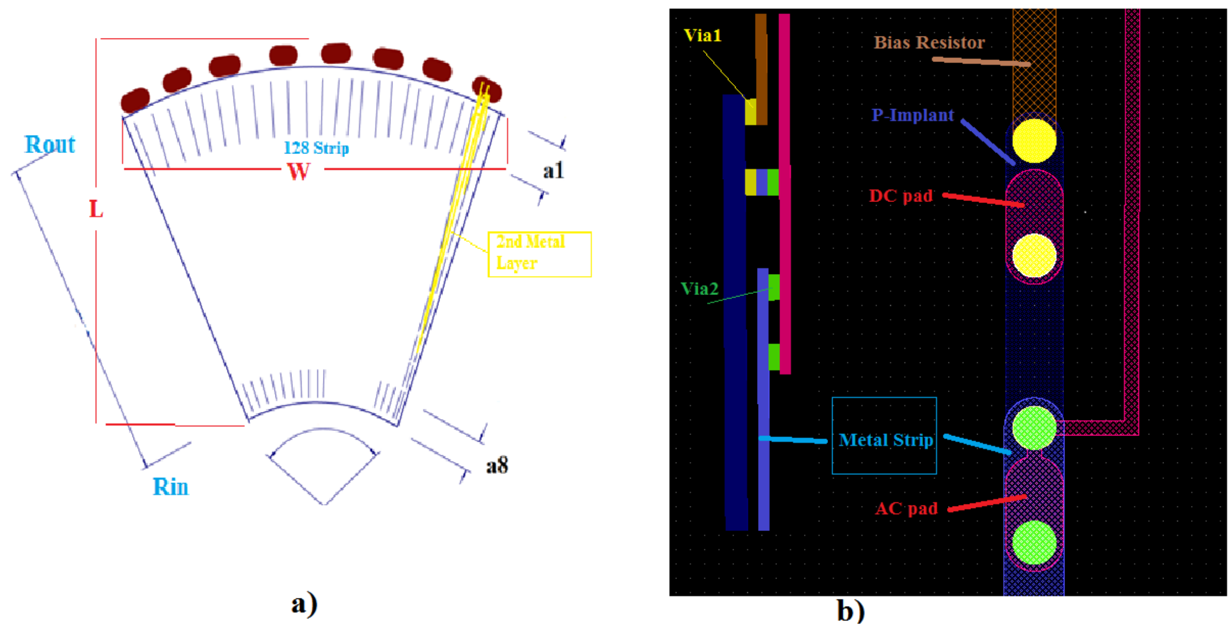

Figure 2 a) General Schematics of Silicon strip module b) Silicon strip layers and cross section